AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1] with the following new paragraph:

[1] The present invention is directed towards a systolic memory array (SMA) and more particularly to a systolic memory array (SMA) that enables the access of memory arrays that are subdivided into a plurality of banks and these banks may be accessed in a pipelined manner.

Please replace paragraph [6] with the following new paragraph:

[6] The various exemplary embodiments of the present invention permits memory arrays subdivided in banks to be accessed in a pipelined fashion. This approach achieves a much higher sustainable memory bandwidth and possibly a shorter average access time than what the individual ~~banks' provides~~ banks provide if they were accessed with shared non-pipelined buses. This design also alleviates the problem of driving long global bit lines in larger memories. Read access of this type of pipelined memory will exhibit physical locality properties and have variable latency. Banks that are located closer to an access port will have shorter access time than banks that are located farther away. Additionally, systolic memories are easier to implement because of their modular designs and they are also more cost effective to produce because of this modular ~~characteristics~~ characteristic.